

Please amend the claims as follows:

Claims 1–9 **(Canceled)**

10. **(Original)** A semiconductor device wherein four memory capacitors are arranged into a substantially cross shape around a bit line contact, and each of said four memory capacitors can be connected to said bit line contact.

11. **(Original)** A semiconductor device comprising:
a bit line contact;
four memory capacitors formed around said bit line contact; and
four gate electrodes formed between said four memory capacitors and said bit line contact,
wherein each of said four memory capacitors and said bit line contact can be connected or disconnected by changing a voltage to be applied to a corresponding one of said four gate electrodes.

12. **(Original)** A device according to claim 11, wherein said memory capacitors are trench capacitors formed in a silicon substrate.

13. **(Original)** A device according to claim 11, wherein
at least two of said four gate electrodes are formed on a predetermined surface, and
the other two of said four gate electrodes are formed below the predetermined surface.

14. **(Original)** A device according to claim 13, wherein
an insulating layer is formed on the side walls of said gate electrodes formed on the predetermined surface, and
said bit line contact is formed in contact with said insulating layer.

15. **(Original)** A semiconductor device comprising:
a bit line contact;
a plurality of gate electrodes formed around said bit line contact; and
a plurality of memory capacitors formed around said bit line contact,
wherein each of said plurality of memory capacitors and said bit line contact
can be connected or disconnected by changing a voltage to be applied to a
corresponding one of said plurality of gate electrodes, and
at least one of said plurality of gate electrodes is formed on a predetermined
surface, and the other of said plurality of gate electrodes is formed below the
predetermined surface.
16. **(Original)** A device according to claim 15, wherein
an insulating layer is formed on the side walls of said gate electrode formed
on the predetermined surface, and
said bit line contact is formed in contact with said insulating layer.
17. **(Original)** A device according to claim 15, wherein said memory capacitors
are trench capacitors formed in a silicon substrate.
18. **(Currently Amended)** A device according to claim 17, wherein said trench
capacitors ~~are trench capacitors according to claim 1~~ comprise:
a trench formed in a surface portion of a semiconductor substrate;
an insulating layer formed on the inner wall surfaces of said trench; and
an electrode portion formed inside said trench having said insulating layer,
and
said electrode portion has a metal portion.
19. **(Original)** A device according to claim 15, wherein said gate electrodes
have a metal interconnection layer.

20. **(Original)** A method of fabricating a semiconductor device in which a plurality of trench capacitors are formed around a bit line contact, and each of said plurality of trench capacitors can be connected to or disconnected from said bit line contact, comprising the steps of:

forming said plurality of trench capacitors on a semiconductor substrate;

forming some of a plurality of gate electrodes each for performing switching for a corresponding one of said plurality of trench capacitors, such that said some gate electrodes are buried in the surface of said substrate;

forming the remaining ones of said plurality of gate electrodes on the surface of said substrate so as to be substantially perpendicular to said some gate electrodes;

covering the side surfaces of said remaining gate electrodes with an insulating layer; and

forming said bit line contact in contact with said insulating layer.